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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,641	12/04/2003	Ming-Dou Ker	6720.0117-00	6205

43831 7590 06/16/2008

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EXAMINER	
BAUER, SCOTT ALLEN	

ART UNIT	PAPER NUMBER
2836	

MAIL DATE	DELIVERY MODE
06/16/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/726,641	KER ET AL.	
	Examiner	Art Unit	
	SCOTT BAUER	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4,28,31,44,48-50,54,60,61 and 65-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4,28,31,44,48-50,54,60,61 and 65-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 4, 31, 48, 54 & 60 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In examining the amended claims, it is believed that the most recent claim amendments add new matter which was not contained within the specification or drawings at the time of the filing.

It is believed that the remaining claims in the application are drawn to the embodiments of Figs. 5A & 5B. The claims are directed to an interface circuit board having: a first surface opposite a second surface; a plurality of first contact receptacles of a first depth on said first surface, at least one of the first contact receptacles including a first end connected to the interface circuit board and a second end to connect to an external device; and: at least two second contact receptacles of a second depth on said first surface, wherein the at least two second contact receptacles include one contact receptacle connected to a first voltage line of a first voltage level, and another contact

receptacle connected to a second voltage line of a second voltage level; and a plurality of pins on said second surface, the plurality of pins adapted to be coupled to integrated circuit contact points, wherein said plurality of pins includes one or more pins that are longer in length than the other pins.

The only embodiments wherein a board with two surfaces contains contacts on a first side and pins on an opposite side are the test head embodiment of Figs. 5A & 5B. The embodiments of Figs. 1 & 2 teach that the side opposite the contacts (32 & 34) and pins (12 & 14) are connected to a board holding an integrated circuit, but make no mention of how the device is coupled to the board. The interface board (104) of Fig. 5 clearly has contacts (104 -6) on a first side (104-2) and pins (120) on an opposite side (104-4). The specification and drawings show that pins (110 & 110') can be different lengths or that pins (120 & 120') can be different lengths. However, the drawings and specification do not teach that the contacts (104-6) have first and second depths. The specification teaches that square contacts are formed on a surface to receive the pins 110 (page 18 paragraph 051). The pins (110) are pogo pins; meaning that a spring action occurs when they are placed on the contacts which are formed on the surface of the board (104) (page 17 paragraph 050). One of ordinary skill in the art would recognize that in a test head environment, pogo pins are coupled to flat contacts mounted on a surface and would not be used to be inserted into a hole with a certain depth.

As such, the recitation of a board with first and second surfaces having contacts of first and second depths on a first side and pins of first and second lengths on an

opposite side is new matter. If the interpretation of the amended claims as given by the Examiner are incorrect, an explanation of where support in the specification or the drawing can be found would be helpful.

2. Claims 4, 28, 31, 44, 48, 54, 60 & 65 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicants have amended the claims to overcome the previous rejection by stating that the "board" of the previous Action is now a "circuit board". However, no where in the drawings or specification can support for the amended claim language be found. Again, it is believed that all claims remaining in the application are directed to the embodiments of Figs. 5A & 5B. While it teaches that the interface circuit (104) is a board, no mention is ever given stating that the board is a circuit board. The only part of the specification wherein circuit boards are expressly mentioned is in the prior art section on page 3 in paragraph 008. The prior art section makes no mention of pins or contacts of first and second lengths or depths respectively being placed on the circuit board. The specification mentions that the connectors of Fig 1 are attached to a board which holds an integrated circuit on the side opposite the pins or sockets (Page 6 paragraph 016). One of ordinary skill in the art would recognize that this board would most likely be a circuit board, however, the pins are mounted on the device 16 or 36

and not on the board, and the board does not have pins and contacts on opposite sides of each.

Based on Figs. 3 & 4, one of ordinary skill in art would assume that boards 50 & 70 are circuit boards. However, the present claims do not describe the embodiments of these figures. Further, these boards do not have pins and contacts on opposite sides of the circuit board.

As stated above, it is believed that Fig. 5 is represented by the claims. There is nothing shown in the specification that board 102 or board 104 comprises a circuit board. It is believed that the circuit board recited in the claims is referring to the interconnecting board 104. The specification refers to the board (104) simply as an interconnect board and makes no mention of any circuits found within the board. The board could be constructed of any material so long as it allows the contacts (104-6) to be in electrical communication with the pins (120). The board 104 is never disclosed as being a circuit board in either the specification or the drawings. Again, if the interpretation of the amended claims as given by the Examiner are incorrect an explanation of where support in the specification or the drawing can be found would be helpful.

The remaining dependant claims 49, 50, 61 & 66-72 are rejected in that they depend from claims that fail to comply with the written description requirement.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4, 31 & 70-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagawa et al. (US 6,348,810), in view of Ogata (US 6,466,450) and Park et al. (US 5,662,483).

With regard to claim 4, Yanagawa teaches an apparatus comprising: an interface circuit board (26) having: a first surface opposite a second surface; a plurality of first contact receptacles (32 & 35) of a first depth on said first surface, at least one of the first contact receptacles including a first end (35A & 32A) connected to the interface circuit board and a second end (35B & 35B) to connect to an external device (25); and: and a plurality of pins (33 & 36) on said second surface, the plurality of pins adapted to be coupled to integrated circuit contact points (21), wherein said plurality of pins includes one or more pins that are longer in length than the other pins and wherein the second depth is greater than the first depth such that the second contact receptacles are adapted to contact the external device prior to the first contact receptacles contacting said external device in response to the circuit board being coupled to the external device.

Yanagawa does not teach at least two second contact receptacles of a second depth on said first surface, wherein the at least two second contact receptacles include one contact receptacle connected to a first voltage line of a first voltage level, and another contact receptacle connected to a second voltage line of a second voltage level or wherein said plurality of pins includes one or more pins that are longer in length than the other pins and wherein the second depth is greater than the first depth such that the second contact receptacles are adapted to contact the external device prior to the first contact receptacles contacting said external device in response to the circuit board being coupled to the external device.

Ogata, in Figure 6, teaches a connector comprising a plurality of pins (34) including one or more pins (34A) that are longer in length than the other pins (34B).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanagawa with Ogata, by ensuring that all of the pins 31 & 34 of Yanagawa shown in Fig. 1 that are used to supply power are longer than the pins which supply a signal, for the purpose of ensuring that all circuits are in a stable state prior to applying a signal voltage thus preventing a malfunction of the circuit (Ogata column 6 lines 24-37).

Park, in Figure 4, teaches a connecting device comprising first (54) and second (53) contact receptacles of a first and second depth on said first surface, wherein the second contact receptacles include one contact receptacle connected to a first voltage line of a first voltage level, and another contact receptacle connected to a second voltage line of a second voltage level wherein the second depth is greater than the first

depth such that the second contact receptacles are adapted to contact the external device prior to the first contact receptacles contacting said external device in response to the circuit board being coupled to the external device (See abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanagawa with Park, by making the sockets on the bottom of circuit board 26 of Yanagawa have first and second depths corresponding to the pins use of a power pin or a signal pin, for the purpose of preventing voltage surges should the interface circuit be inadvertently disconnected from the test head when voltage is still being applied (Ogata abstract).

With regard to claims 70 & 72, Yanagawa in view of Ogata and Park discloses the device of claim 4. Yanagawa in view of Ogata and Park further discloses that the first voltage level is VSS and the second voltage level is VDD or VCC (as taught by both Ogata & Park) (re claim 70), wherein the first surface and the second surface of the interface circuit board are parallel to one another and able to connect the external device (25) and the integrated circuit contact points (21), the external device and the integrated circuit contact points being parallel to one another when connected to one another via the interface circuit board (as seen in fig 3 of Yanagawa) (re claim 72).

With regard to claims 31 & 71, Yanagawa in view of Ogata and Park discloses a method, comprising: providing an interface circuit board (26 Yanagawa), the device including: a first surface opposite a second surface: a plurality of first contact

receptacles (32b & 34B) of a first depth on said first surface, at least one of the first contact receptacles including a first end connected to the board and a second end to connect to an external device (25) ; and at least two second contact receptacles of a second depth on said first surface (As taught by Park), wherein the at least two second contact receptacles include one connected to a first voltage line of a first voltage level, and another connected to a second voltage line of a second voltage .level; and providing a plurality of pins on said second surface, the plurality of pins (31 & 34) adapted to be coupled to integrated circuit contact points (21), wherein said plurality of pins includes one or more pins that are longer in length than the other pins (as taught by Ogata) and wherein the at least two second contact receptacles have a depth greater than the depth of at least one of the first contact receptacles to discharge electric charges accumulated on the board via the at least two second contact receptacles the circuit board is coupled to the external device (as taught by Park) (re claim 31), wherein the first voltage level is VSS and the second voltage level is VDD or VCC (as taught by Park and Ogata).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanagawa with Ogata and Park, as described above.

4. Claims 28, 44, 48-50 & 65-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagawa in view of Takagi (US 5,969,533) and Ogata.

With regard to claim 28, Yanagawa teaches a system, comprising: a plurality of first pins (27) attached a first circuit board (25); a second circuit board (26) including a first surface opposite a second surface; a plurality of first contact points (32B & 35B) formed on the first surface of the second circuit board to receive the first pins; and a plurality of second pins (31 & 34) formed on the second surface of the second circuit board, the plurality of second pins adapted to be coupled to integrated circuit contact points (21).

Yanagawa does not teach that the first set of pins are formed on a first circuit board, and rather that the first set of pins (27) are provided by a cable that interconnects the first and second circuit boards or that the plurality of first pins includes one or more first pins that are longer in length than the other first pins, or the plurality of second pins includes one or more second pins that are longer in length than the other second pins.

Takagi (US 5,969533) in Fig. 5 teaches a test head assembly wherein the test head circuit board (3) has pogo pins directly formed on the circuit board which connect to the interface board.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanagawa with Takagi, by coupling the interface circuit directly to the test head instead of using cables, for the purpose of reducing the length that the signals are required to travel thus reducing the chance of noise and cross talk between signals.

Ogata, in Figure 6, teaches that a plurality of first pins (34) includes one or more first pins (34A) that are longer in length than the other first pins (34B).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanagawa with Ogata, by ensuring that all of the pins 31 & 34 of Yanagawa shown in Fig. 1 that are used to supply power are longer than the pins which supply a signal, for the purpose of ensuring that all circuits are in a stable state prior to applying a signal voltage thus preventing a malfunction of the circuit (Ogata column 6 lines 24-37).

With regard to claim 44, Yanagawa in view of Takagi and Ogata discloses a method, comprising: providing a test device including a first circuit board (25), the first circuit board including a plurality of first pins (27) (as taught by Takagi); providing a second board (26) including a first surface opposite and a second surface, the second circuit board including a plurality of first contact points (32b & 35b) on the first surface to receive the first pins, and a plurality of second pins (31 & 34) on the second surface, wherein at least one of the first pins is longer than the other first pins (as taught by Ogata), or at least one of the second pins is longer than that of the other second pins; and providing a plurality of second contact points on a plurality of integrated circuits (21) to receive the second pins to discharge electric charges accumulated on a third circuit board on which the integrated circuits are formed if the first pins are coupled to the first contact points and the second pins to the second contact points.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanagawa with Takagi and Ogata, as described above.

With regard to claims 48-50, Yanagawa in view of Takagi and Ogata discloses a system, comprising: a plurality of first pins (27) formed on a first circuit board (25) (as taught by Takagi); a second circuit board (26) including a first surface opposite a second surface; a plurality of contact receptacles (32b & 35b) formed on the first surface of the second circuit board to receive the first pins; and a plurality of second pins (31 &34) formed on the second surface of the second circuit board, wherein the plurality of contact receptacles includes one or more contact receptacles that are deeper than the other contact receptacles, or the plurality of second pins includes one or more second pins that are longer in length than the other second pins (as taught by Ogata) (re claim 48), wherein the plurality of second pins are adapted to be coupled to integrated circuit contact points (21) re claim 49), wherein all of the first pins have equal lengths (as seen in Fig. 2 of Yanagawa) (re claim 50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanagawa with Takagi and Ogata, as described above.

With regard to claims 65 - 69, Yanagawa in view of Takagi and Ogata teaches an apparatus, comprising: a circuit board (25) for an integrated circuit tester, the circuit board including a surface having a plurality of contact pins (27) (as taught by Takagi) of a first length and at least one contact pin of a second length longer than the first length (as taught by Ogata); a second circuit board (26) including a first surface opposite a

second surface; a plurality of first contact points (32b & 35b) formed on the first surface of the second circuit board to receive the contact pins; and a plurality of second pins (31 & 34) formed on the second surface of the second circuit board, the plurality of second pins adapted to be coupled to integrated circuit contact points(21) (re claim 65), wherein the board comprises one of an interface board or an interconnect board (see fig. 5 Takagi) (re claim 66), wherein the plurality of contact pins of a first length and the at least one contact pin of a second length comprise pogo pins (9 of Takagi and 31 & 34 of Yanagawa) (re claim 67), wherein the plurality of contact pins of a first length are adapted to contact input/output terminals of an integrated circuit mounted (21) on the second board, and wherein the at least one contact pin of the second length is adapted to discharge current from the second board (as taught by Ogata) (re claim 68), wherein the plurality of contact pins (27) of the first length are adapted to contact contact points of the second board (32b & 35b), and wherein the at least one contact-pin of the second length is adapted to discharge current from the second board (as taught by Ogata) (re claim 69).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanagawa with Takagi, as described above.

5. Claims 54, 60 & 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagawa in view of Takagi and Park.

With regard to claim 54, Yanagawa teaches a detecting system, comprising: a plurality of first pins (27) coupled a test head (25); an interconnect circuit board (26) including a first surface opposing and a second surface; a plurality of contact receptacles (32b & 35b) formed on the first surface of the interconnect circuit board to receive the first pins; and a plurality of second pins (31 & 34) formed on the second surface of the interconnect circuit board,. wherein the plurality of contact receptacles includes one or more contact receptacles that are deeper than the other contact receptacles, so that the one or more contact receptacles are adapted to contact the first pins prior to the other contact receptacles contacting the first pins in response to the test head being coupled to the interconnect circuit board.

Yanagawa does not teach that the first pins are formed on the first board or that wherein the plurality of contact receptacles includes one or more contact receptacles that are deeper than the other contact receptacles, so that the one or more contact receptacles are adapted to contact the first pins prior to the other contact receptacles contacting the first pins in response to the test head being coupled to the interconnect circuit board.

Takagi (US 5,969533) in Fig. 5 teaches a test head assembly wherein the test head circuit board (3) has pogo pins directly formed on the circuit board which connect to the interface board.

Park, in Figure 4, teaches a connecting device comprising first (54) and second (53) contact receptacles of a first and second depth on said first surface, wherein the second contact receptacles include one contact receptacle connected to a first voltage

line of a first voltage level, and another contact receptacle connected to a second voltage line of a second voltage level wherein the second depth is greater than the first depth such that the second contact receptacles are adapted to contact the external device prior to the first contact receptacles contacting said external device in response to the circuit board being coupled to the external device (See abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yanagawa with Takagi and Park as described above.

With regard to claims 60 & 62, Yanagawa in view of Takagi and Park discloses a method, comprising: arranging a test head (25) having a plurality of first pins (27) adjacent to an interconnect circuit board (26) (as taught by Takagi) that includes a first surface opposite and a second surface, the first surface including a plurality of contact receptacles (32b & 35b), and the second surface including a plurality of second pins (31 & 34); and coupling the test head to the interconnect circuit board so that the contact receptacles receive the first pins, wherein the plurality of contact receptacles includes one or more contact receptacles that are deeper than the other contact receptacles, so that the one or more contact receptacles are adapted to contact the first pins prior to the other contact receptacle contacting the first pins in response to the test head being coupled to the interconnect circuit board (as taught by Park) (re claim 61) and further comprising connecting the second pins to a board that includes integrated circuits (21)

(re claim 62).

Response to Arguments

Applicant's arguments filed 02/13/2008 have been fully considered but they are not persuasive. Applicant's argue that the rejection found in the previous action have been overcome because the claims have been amended. The amended claims have been newly rejected and so the arguments are moot. The new rejection of each claim was necessitated by the amendment as all claims were amended to include new matter. The new obviousness type rejections found in the present action were necessitated by amendment as well.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SCOTT BAUER whose telephone number is (571)272-5986. The examiner can normally be reached on M-F 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J Sherry/
Supervisory Patent Examiner, Art Unit 2836

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